WHAT IS CLAIMED IS:

1. An image processor with frame-rate conversion that generates video signals being rate-converted by converting a vertical synchronization frequency of input digital video signals consisting of successive frames into a desired frequency, said image processor comprising:

a frame memory having a storage capacity for a single frame of said input digital video signals;

a memory write control circuit which successively writes said input digital video signals on said frame memory with a timing synchronized with a vertical synchronization signal included in said input digital video signals;

a vertical synchronization signal generating circuit which produces a frequency signal mainly consisting of a train of N pulses (N being a natural number) for every M cycles (M being a natural number) of the vertical synchronization signal, as a vertical synchronization signal being rate-converted, the natural number N being larger than the natural number M; and

a memory readout control circuit which reads out and outputs the input digital video signals from said frame memory in the order in which said input digital video signals were written and with a timing synchronized with the vertical synchronization signal being rate-converted, as said video signals being rate-converted.

2. An image processor with frame-rate conversion according

to claim 1, wherein the natural number N is smaller than two times the natural number M.